Amendments to the Claims:

This listing of claims will replace all prior versions, and listings of claims in the application:

Listing of Claims:

Claim 1.- 2. (canceled)

Claim 3. (previously presented) A programmable logic device, comprising:

an active logic section and a configuration memory, wherein the active logic section and the configuration memory have separate power supply connections, wherein the active logic section comprises a gate array; and wherein the active logic section further comprises an embedded logic device, and the gate array and the embedded logic device have separate power supply connections.

Claim 4. (original) A programmable logic device as claimed in claim 3, wherein the logic device comprises an embedded processor.

Claim 5. (currently amended) A programmable logic device, comprising:

an active logic section and a configuration memory, wherein the active logic section and the configuration memory have separate power supply connections; and further comprising a programmable input/output section, wherein the programmable input/output section has a further separate power supply connection, wherein each of the separate power supply connections for the active logic section, the configuration memory, and the programmable input/output section are selectable between at least two different voltage levels.

Claim 6. (currently amended) A programmable logic device, comprising:

an active logic section and a configuration memory, wherein the active logic section and the configuration memory have separate power supply connections; and wherein ~~the configuration memory has power supply connections to power supplies at two different voltages~~ the separate power supply connections are selectable between a first voltage level and a second voltage level lower in value than the first voltage level.

Claim 7.- 8. (canceled)

Claim 9. (previously presented) A programmable logic device integrated circuit, having a plurality of pins for connection to respective other devices, the programmable logic device integrated circuit comprising:

an active logic section and a configuration memory, wherein the active logic section is connected to at least a first pair of said pins to receive power therefrom, and the configuration memory is connected to a second pair of said pins different from the first to receive power therefrom, wherein the active logic section comprises a gate array, wherein the active logic section further comprises an embedded logic device, and the gate array is connected to said first pair of said pins to receive power therefrom, and the embedded logic device is connected to a third pair of said pins different from the first to receive power therefrom.

Claim 10. (original) A programmable logic device integrated circuit as claimed in claim 9, wherein the embedded logic device further comprises an embedded processor.

Claim 11. (previously presented) A programmable logic device integrated circuit, having a plurality of pins for connection to respective other devices, the programmable logic device integrated circuit comprising an active logic section and a configuration memory, wherein the active logic section is connected to at least a first pair of said pins to receive power therefrom, and the configuration memory is connected to a second pair of said pins different from the first to receive power therefrom, further comprising a programmable input/output section, wherein the programmable input/output section is connected to a fourth pair of said pins different from the first and second to receive power therefrom.

Claim 12. (canceled)

Claim 13. (previously presented) In a programmable logic device, comprising:

an active logic section and a configuration memory, a method comprising operating the device in a first mode of operation, in which power is supplied to the configuration

memory and power is disconnected from the active logic section, wherein the active logic section comprises a gate array and an embedded logic device, the method further comprising operating the device in a second mode of operation, in which power is supplied to the gate array of the active logic section and power is disconnected from the embedded logic device.

Claim 14. (currently amended) In a programmable logic device, comprising an active logic section and a configuration memory, a method comprising:

operating the device in a first mode of operation, in which power is supplied to the configuration memory and power is disconnected from the active logic section, wherein the programmable logic device further comprises a programmable input/output section, wherein, in the first mode of operation, power is supplied to the programmable input/output section, wherein the power supplied to the configuration memory or to the programmable input/output section comprises at least two selectable voltage levels.

Claim 15. (currently amended) In a programmable logic device, comprising:

an active logic section and a configuration memory, a method comprising operating the device in a first mode of operation, in which power is supplied to the configuration memory and power is disconnected from the active logic section, the method further comprising operating the device in a normal mode of operation, in which power is supplied to the configuration memory and to the active logic section, wherein the power supplied to the active logic section or to the programmable input/output section comprises at least two selectable voltage levels.

Claim 16. (original) A method as claimed in claim 15, the method further comprising supplying a first voltage to the configuration memory in said normal mode of operation and supplying a second voltage, lower than said first voltage, to the configuration memory in said first mode of operation.

Claim 17. (previously presented) In a programmable logic device, comprising:

an active logic section and a configuration memory, a method comprising operating the device in a first mode of operation, in which power is supplied to the configuration memory and power is disconnected from the active logic section, further comprising:

before entering said first mode of operation, storing data from registers of said active logic section in a memory device separate from said programmable logic device; and

after completing said first mode of operation retrieving said data, stored in said separate memory device, into the registers of said active logic section.

Claim 18. (canceled)

Claim 19. (previously presented) An electronic device comprising:

a power supply and a programmable logic device integrated circuit, wherein the power supply comprises a plurality of power supply rails, and the programmable logic device integrated circuit comprises an active logic section and a configuration memory, wherein the active logic section is connected to a first pair of said power supply rails through a first pair of said pins on said integrated circuit to receive power therefrom, and the configuration memory is connected to a second pair of said power supply rails through a second pair of said pins different from the first to receive power therefrom, wherein the power supply comprises a plurality of power supply rails at different respective voltages, and the active logic section and the configuration memory are connected to power supply rails at different respective voltages.

Claim 20. (canceled)

Claim 21. (previously presented) An electronic device comprising:

a power supply and a programmable logic device integrated circuit, wherein the power supply comprises a plurality of power supply rails, and the programmable logic device integrated circuit comprises an active logic section and a configuration memory, wherein the active logic section is connected to a first pair of said power supply rails through a first pair of said pins on said integrated circuit to receive power therefrom, and the configuration memory is connected to a second pair of said power supply rails through a second pair of said pins different from the first to receive power therefrom, wherein the active logic section of the programmable logic device integrated circuit comprises a gate array, wherein the active logic section of the programmable logic device integrated circuit further comprises an embedded logic device, and the gate array is connected to said first pair of said pins on said integrated circuit to receive power therefrom, and the embedded logic device is connected to a third pair of said pins on said integrated circuit different from the first pair to receive power therefrom.

Claim 22. (previously presented) An electronic device comprising:

a power supply and a programmable logic device integrated circuit, wherein the power supply comprises a plurality of power supply rails, and the programmable logic device integrated circuit comprises an active logic section and a configuration memory, wherein the active logic section is connected to a first pair of said power supply rails through a first pair of said pins on said integrated circuit to receive power therefrom, and the configuration memory is connected to a second pair of said power supply rails through a second pair of said pins different from the first to receive power therefrom, wherein the programmable logic device integrated circuit further comprises a programmable input/output section, and wherein the programmable input/output section is connected to a fourth pair of said pins on said integrated circuit different from the first and second pairs to receive power therefrom.

Claim 23. (original) An electronic device as claimed in claim 19, wherein said configuration memory is connected to power supply rails at two different voltages.

Claim 24. (original) An electronic device as claimed in claim 23, wherein, when the active logic section is connected to said first pair of said power supply rails through said first pair of said pins on said integrated circuit to receive power therefrom, the configuration memory is connected to said second pair of said power supply rails through said second pair of said pins different from the first to receive power therefrom, and, when the active logic section is disconnected from said first pair of said power supply rails, the configuration memory is connected to a third pair of said power supply rails through a fifth pair of said pins to receive power therefrom at a reduced voltage.

Claim 25. (original) An electronic device as claimed in claim 24, further comprising a memory device, wherein, when said active logic section is to be disconnected from said first pair of said power supply rails, data stored in registers of said active logic section is transferred to said memory device.

Claim 26. (previously presented) A programmable logic circuit comprising:

an active logic section having a selectable power supply connection;

a configuration memory having a selectable power supply connection;

a gate array having a selectable power supply connection;

a power control circuit configured to operate each of the selectable power supply connections to selectively supply different power supply voltages to the active logic circuit, the configuration memory, and the gate array in response to a predetermined mode of operation.

Claim 27. (previously presented) The programmable logic circuit of claim 26, wherein the different power supply voltages comprise power supply rails that each provide a different power supply voltage to the programmable logic circuit.

Claim 28. (previously presented) The programmable logic circuit of claim 26, wherein each of the selectable power supply connection comprises at least one switch operable by the power control circuit.

Claim 29. (previously presented) The programmable logic circuit of claim 26, wherein when the mode of operation is a low power mode, the power control circuit connects a reduced voltage to the configuration memory and connects no power to the gate array.

Claim 30. (previously presented) The programmable logic circuit of claim 26, wherein when the mode of operation is a low power mode, the power control circuit connects a voltage to one or more input/output blocks but does not supply a voltage to the gate array or to the configuration memory.

Claim 31. (previously presented) The programmable logic circuit of claim 30, wherein the power control circuit provides an enable signal to one or more input/output blocks to maintain a state of the input/output blocks with respect to power supplied to the gate array.

Claim 32. (previously presented) The programmable logic circuit of claim 30, wherein the enable signal is asserted to maintain a state of the input/output blocks when the gate array is supplied no power.

Claim 33. (previously presented) The programmable logic circuit of claim 30, wherein the enable signal is de-asserted to allow a state change of the input/output blocks when the gate array is supplied power.